REMARKS

Claim 7 has been amended, and claim 14 added to the application. The attachment to this Amendment entitled "Version with Markings to Show Changes Made" in a marked-up version of the changes made to the claims. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

1. In the Office Action on page 2 in section 2, claim 7 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for reciting "the said" on line 4. Claim 7 has been amended accordingly. Claim 7 has additionally been amended to correct two typographical errors.

2. In the Office Action on pages 2-4 in section 4, claims 1-6 and 8-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,430,718 to Petersen (hereinafter Petersen). Applicant respectfully traverses this rejection.

The invention of the application teaches a switching mechanism where TDM and packet data are switched by a single shared memory mechanism such that switching packet data has no latency or jitter effect on the TDM traffic. See, e.g., specification, page 5, 14-24. TDM and packet shared memory partitions and packet data queues per port contribute to the lack of latency or jitter effect on the TDM traffic. A varying amount of shared memory is used to store packet data, whereas the TDM portion of the shared memory is constant. Additionally, the use of routing information stored as part of a data exchange unit (DEU) assists in routing packet data.

The switching of packet data by the shared memory has no latency or jitter effect on the switching of TDM data by the shared memory.

Claim 1 recites a switch for switching TDM data and packet data from input ports to output ports. The switch comprises a plurality of input ports, a plurality of output ports, and a shared memory. The plurality of input ports receive data, and each data comprises either TDM data or packet data. The plurality of output ports transmit switched data. The shared memory couples the input ports to the output ports and sequentially receives the data from the input ports. The shared memory switches a sequentially received data from a respective input port to a respective output port. The switching of packet data by the shared memory has no latency or jitter effect on switching of TDM data by the shared memory.

Petersen teaches a switch that passes data between transmitting and receiving devices when there is a desired association (e.g. a "call" or a valid "connection") between the two devices. When no connection is desired, Petersen teaches the generation of "idle" codes to be sent to the receiving device in lieu of actual data from the transmitting device. Petersen, column 2, lines 2-8. Petersen, however, fails to teach at least two aspects of claim 1.

First, Petersen fails to teach switching packet data. Petersen teaches in Figure 2 a switch memory 4 for switching TDM time slots between input ports of a multiplexer 12S and output ports of a multiplexer 12M. Petersen, column 2, lines 38-40 and 57-59; column 3, lines 30-32. The switching is performed in the **TDM domain** with **no** special provisions for the switching of packet data. Petersen, column 2, lines 51-64; column 3, lines 11-13. Petersen describes his invention as being used as a circuit switch but fails to describe his invention as being used for packet switching. Compare Petersen, column 1, lines 5-7, column 3, lines 38-40 (invention only used for circuit switched data) and Petersen, column 1, lines 43-45 and 58-60 (prior art used for

circuit switched data and packet data). In fact, **nowhere** does Petersen even mention the switching of TDM data **and** packet data through the switch memory 4. Further, Petersen fails to consider the additional requirements needed for switching packet data, such as the need for queuing of packet data. Hence, Petersen fails to teach switching packet data.

Second, Peterson fails to teach the avoidance of latency or jitter effects on the switching of TDM data by a shared memory due the switching of packet data by the shared memory. Because Petersen fails to teach or even acknowledge the switching of packet data by the shared memory 4, Petersen fails to disclose that the switching of packet data may affect the switching of TDM data by the switch memory 4. Petersen teaches switching TDM traffic between input devices 10S and output devices 10N with no consideration for the special processing required of the traffic packet data. Petersen column 2, lines 51-64; column 3, lines 30-32. The only concern of Petersen is whether the connections to the devices 10M are valid or not valid. Petersen column 3, lines 33-40; column 3, line 64, to column 4, line 9. Petersen fails to appreciate the need to avoid the impact of packet processing on TDM latency or jitter and fails to disclose that the switching of packet data by a shared memory has no latency or jitter effect on switching of TDM data by the shared memory.

Claims 2-6 and 8-9 are dependent from claim 1 and are allowable as being dependent from an allowable claim.

Further, claim 3 recites that the shared memory comprises a TDM data memory portion and a packet data memory portion. This aspect of the invention supports the implementation of specific packet switching processing independent from TDM switching processing. Particularly, with the partitioned memory, packet queues and shared memory specifically for packet switching processing can be implemented. See, e.g., specification page 9, lines 25-28; page 10, lines 22-

25. In contrast, Petersen fails to teach partitioning the switch memory 4. Specifically, Petersen teaches using the switch memory 4 as a **contiguous block** of memory to store **all** incoming data, where the **entire** switch memory 4 is updated once per frame. Petersen, column 2, lines 51-64. Hence, Petersen fails to teach a partitioned shared memory.

Claim 4 recites that the shared memory treats the input ports as logical input ports. As discussed in the application, the physical switch input ports can be segmented into "logical input ports." See, e.g., specification, page 7, lines 18-22. A single physical port can encapsulate many logical ports. For example, referring to Figure 6 of the application, the physical ports are indicated with 27, and the logical ports are identified with 29. Logical ports are significant with respect to the switching of packet data. Packets can be lengthy and thus easily require a channel capacity greater than that provided by a single time slot. Aggregating time slots on a physical port into logical ports facilitates the switching and queuing of packet data as well as separate treatment of packet data from TDM data. See, e.g., specification, page 7, 23-29. In contrast, Petersen fails to teach logical input ports. Instead, Petersen teaches individual transmitter devices 10S sourcing data to be switched. Petersen, column 2, lines 54-64. Each device 10S1 through 10Sn corresponds to a **physical port** into the switch memory 4 and does **not** correspond to a logical input port. Hence, Petersen fails to teach logical input ports.

Claim 5 recites that the shared memory places sequentially received packet data in a queue for a respective output port. In contrast, Petersen fails to teach any usage of packet data queues in the switch memory 4. Instead of teaching packet data queuing, Petersen teaches TDM time slot switching on a frame basis **without** queues. Petersen, column 2, lines 51-64; column 3, lines 11-13 and 30-32. The switch memory 4 of Petersen holds a single TDM frame, and the time that the TDM spends in the switch memory 4 is constant at one frame. Petersen, column 2,

lines 54-64. In contrast, a queue causes a variable switching time delay that is neither contemplated nor accommodated by Petersen. Hence, Petersen fails to teach a queue for packet data.

Claim 6 recites that the data received by the input ports and transmitted by the output ports are data exchange units. See, e.g., specification, page 5, line 5, to page 6, line 9. For packet data, the data exchange units can include header information. See, e.g., specification, page 12, lines 18-29. In contrast, Petersen fails to mention or even refer to the concept of "exchange units" or "data exchange units." Instead, Petersen teaches the usage of a time slot counter 2 in Figure 2 to write data to the switch memory 4. Petersen, column 2, lines 51-54. Petersen further teaches in Figure 2 the control memory 18 and the time slot counter 2 controlling the readout of the switch memory 4 once per frame. Petersen, column 2, line 65, to column 3, line 2. Additionally, Petersen fails to teach the use of such control information **within the time slot data itself** to control the writing of the data into and reading of the data out of the switch memory 4 as well as between the input ports and the output ports. The recited data exchange units are **not** the same as the time slots of Petersen. Hence, Petersen fails to teach data exchange units.

3. In the Office Action on pages 4-5 in section 6, claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Petersen in view of U.S. Patent No. 4,731,785 to Ferenec et al. (hereinafter Ferenec). Applicant respectfully traverses this rejection.

Claim 7 is dependent from claim 1 and is allowable as being dependent from an allowable claim.

Further, claim 7 recites the switch further comprising a time slot interchange controller and a packet switch controller. The time slot interchange controller is coupled to the shared memory and selects an address of the shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data. The packet switch controller is coupled to the shared memory and selects an address in the shared memory to store packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

In rejecting claim 7, the Office Action acknowledges that Petersen fails to teach either a time slot interchange controller or a packet switch controller. To overcome the deficiencies of Petersen the Office Action relies on the teachings of Ferenec. Ference, however, fails to teach either a time slot interchange controller or a packet switch controller.

First, Ferenec does not teach a time slot interchange controller for switching TDM data based on a time slot of a frame. The recited invention uses a time slot of a frame for switching TDM data. See, e.g., specification, page 9, lines 1-8; page 12, lines 14-17. In contrast, Ferenec teaches **inserting control information** in order to identify TDM traffic. Ferenec, column 2, lines 5-7. Switching based on inserted control information is **not** the same as switching based on a time slot of a frame.

Second, Ferenec fails to teach a packet switch controller for switching packet data based on routing data embedded in the packet data. The recited invention uses routing data embedded in the packet data. See e.g., specification, page 12, lines 18-22. In contrast, Ferenec teaches **inserting a control bit** into the TDM stream to identify and process packet data traffic. Ferenec, column 2, lines 5-7. Inserting a control bit is **not** the same as referring to routing data **embedded**

in the packet. Hence, Ferenec fails to overcome the deficiencies of Petersen, and claim 7 is allowable.

4. In the Office Action on pages 5-7 in section 7, claims 10-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Petersen in view of U.S. Patent No. 4,941,141 to Hayano (hereinafter Hayano). Applicant respectfully traverses this rejection.

Claim 10 recites a method for switching TDM data and packet data from input ports to output ports. The method comprises switching a TDM data from an input port to an output port comprising: receiving a TDM data at the input port; determining the output port to route the TDM data; storing the TDM data in a preselected area of a shared memory; reading the TDM data from the preselected area of the shared memory; and transmitting the TDM data from the output port. The method further includes switching a packet data from an input port to an output port comprising: receiving a packet data at the input port; determining the output port to route the packet data; storing the packet data in the shared memory; reading the packet data from the shared memory; and transmitting the packet data from the output port. Switching the packet data has no latency or jitter effect on switching TDM data.

In rejecting claim 10, the Office Action states that Petersen teaches every limitation of claim 10 except storing and reading TDM data from a preselected area of a shared memory. To overcome the deficiencies of Petersen, the Office Action relies on the teachings of Hayano.

As discussed above for claim 1, Petersen fails to teach, first, switching packet data and, second, switching packet data such that no latency or jitter effect occurs for the switching of TDM data. For the same reasons discussed above for claim 1, claim 10 is allowable over Petersen. In addition, Hayano fails to overcome the deficiencies of Petersen.

Regarding the reliance by the Office Action on Hayano, Hayano fails to teach a shared memory for storing packet data and having a preselected area for storing TDM data. Hayano teaches in Figure 3 using two switch memories 104 and 105 as alternate TDM frame stores to facilitate frame alignment within a single TDM stream. Hayano, column 1, line 61, to column 2, line 2. Using the two switch memories 104 and 105 as frame stores allows two TDM frames to be stored at a time. Hayano, column 2, lines 18-22. The traffic is written into each switch memory 104 and 105 as TDM data and is read out as TDM data. Hayano, however, has **no** teachings regarding packet data or switching packet data. Hayano fails to teach a shared memory having a preselected area storing TDM data that likewise has a capability for storing packet data. Hence, Hayano fails to teach the recited switch memory having a preselected area, and claim 10 is allowable over Petersen in view of Hayano.

Claims 11 and 12 are dependent from claim 10 and are allowable as being dependent from an allowable claim.

Further, claim 12 recites that the output port to which TDM data is routed is determined based on a time slot in a frame in which the TDM data was received by the input port, and that the output port to which the packet data is routed is determined based on routing data embedded in the packet data and based on the input port which received the packet data. In contrast, Petersen fails to teach routing packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Initially, as discussed above for claim 1, Petersen fails to teach switching **packet data**. Further, Petersen teaches using connection status to determine whether a connection is present or not and **sets** an indicator bit 32. Petersen, column 3, lines 64-68. Petersen does not teach routing packet data based on routing data **embedded** in the packet data and the **input port** which received the packet data. Hence,

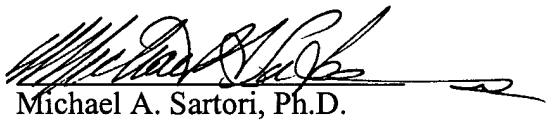
Petersen fails to teach the routing packet data as recited. Additionally, Hayano fails to overcome the deficiencies of Petersen, and claim 12 is thus allowable.

Claim 13 recites subject matter similar to that recited in claim 10 and is allowable for the same reasons discussed above for claim 1.

5. Claim 14 is added to the application and is dependent from claim 1. Claim 14 is allowable as being dependent from an allowable claim.

THEREFORE, because all rejections have been overcome, it is submitted that claims 1-14 are allowable, and such allowance is requested.

Respectfully submitted,



Michael A. Sartori, Ph.D.
Registration No. 41,289
VENABLE
P.O. Box 34385
Washington, DC 20043-9998
Telephone: (202) 926-4800
Telefax: (202) 962-8300

MAS/srb
DC2/314465

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 7 is amended as follows:

7. (Amended) A switch as claimed in claim 1, further comprising:

a time slot interchange controller coupled to said shared memory selecting addresses in said [shard] shared memory to store TDM data, said time slot interchange controller selecting an address of said shared memory for a TDM data based on a time slot of a frame in which [the] said switch received the TDM data; and

a packed switch controller coupled to said shared memory selecting addresses in said [shard] shared memory to store packet data, said packet switch controller selecting an address of shared memory for a packet data based on routing data embedded in the packed data and based on the input which received the packet data.